In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A digital system having a processor comprising a processor pipeline with a plurality of pipeline stages, a plurality of protected resources connected to receive data from certain ones of the plurality of pipeline stages and a pipeline protection mechanism, wherein the pipeline protection mechanism comprises:

a set of shadow registers;

interlock circuitry for anticipating a particular access conflicts for each protected resource of the plurality of protected resources between the pipeline stages, an output of the interlock detection circuitry being controllably connected to the set of shadow registers, the interlock circuitry comprising a stall vector filter, wherein the stall vector filter has a plurality of select filter stages connected in a serial manner such that each of the select filter stages is associated with a corresponding protected resource; and

the set of shadow registers being interconnected with the processor pipeline such that a particular data item from a first pipeline stage can be redirected from a protected resource into a selected shadow register only in response to an the particular access conflict anticipated by the interlock circuitry so that a resource access conflict is resolved without stalling the processor pipeline.

2. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, wherein the interlock circuitry comprises:

interlock detection circuitry operable to anticipate access conflicts for all of the protected resources and the stall vector

filter operable to form a stall vector signal indicative of anticipated access conflicts;

reservation and stall vector filtering circuitry connected to receive the stall vector signal and operable to select an available shadow register from the set of shadow registers in response to the stall vector signal; and

shadow management circuitry connected to the reservation and filtering circuitry, the shadow management circuitry having an output signal controllably connected to the set of shadow registers.

3. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, wherein the interlock circuitry comprises arbitration circuitry for each protected resource such that each arbitration circuit is definable as a specific form of a single, generic arbitration function.

4. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, including pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive the stall control signals output from the interlock circuitry based upon a result of arbitration between resources.

5. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, wherein at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register.

6. (Canceled)

7. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, wherein the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register.

8 to 12. (Canceled)

13. (Previously Amended) The digital system of Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.

14 to 18. (Canceled)

19. (Currently Amended) The ~~processing engine~~ digital system according to Claim 1, wherein the processor pipeline is operable to update periodically, and wherein the interlock circuitry is operable to anticipate access conflicts for each protected resource during each pipeline period prior to each periodic update of the processor pipeline.

20. (Currently Amended) The ~~processing engine~~ digital system according to Claim 19, wherein certain of the plurality of pipeline stages are subject to access conflicts, and wherein the interlock circuitry is connected to receive resource access signals provided by each pipeline stage that is subject to access conflicts, whereby additional control storage circuitry is not required for storing conflict control information.

21. (New) A digital data processor including a processor pipeline with a plurality of pipeline stages and operable upon instructions specifying operands from a plurality of logical registers comprising:

a plurality of physical data registers, each corresponding to fixed respective logical register;

a set of shadow registers;

an interlock detection circuit for anticipating write after read (WAR), write after write (WAW) and read after write (RAW) register access conflicts of instructions between the pipeline stages, said interlock detection circuit generating a stall vector upon detection of a conflict indicating a number of pipeline stages of stall for the detected conflict; and

a register control circuit connected to the plurality of physical registers, the set of shadow register and the interlock detection circuit, the register control circuit operable to

permit an instruction to access logical registers via the corresponding physical data registers in the absence of detection of a register access conflict,

stall an instruction a number of pipeline stages indicated by the stall vector upon detection of a read after write (RAW) register access conflict and thereafter permit the instruction to access logical registers via the physical data registers, and

write data to a shadow register upon detection of a write after read (WAR) or write after write (WAW) register access conflict and following expiration of a number of pipeline stages indicated by the stall vector transfer data from the shadow register to the physical data register corresponding to the logical register of a data destination of the instruction.

22. (New) The digital data processor of claim 21, wherein:

the set of shadow registers is less than a maximum number of instructions that can simultaneously cause register access conflicts of instructions between the pipeline stages; and

the register control circuit is further operable to

write data to a shadow register upon detection of a write after read (WAR) or write after write (WAW) register access conflict if a shadow register is free and following expiration of a number of pipeline stages indicated by the stall vector transfer data from the shadow register to the physical data register corresponding to the logical register of a data destination of the instruction and free the shadow register, and

stall an instruction a number of pipeline stages indicated by the stall vector upon detection of a write after read (WAR) or write after write (WAW) register access conflict if no shadow register is free and thereafter permit the instruction to access logical registers via the physical data registers.

23. (New) A method of data processing in digital data processor including a processor pipeline with a plurality of pipeline stages and operable upon instructions specifying operands from a plurality of logical registers, the method comprising the steps of:

detecting write after read (WAR), write after write (WAW) and read after write (RAW) register access conflicts of instructions between the pipeline stages;

upon detecting a register access conflict generating a stall vector indicating a number of pipeline stages of stall for the detected conflict; and

in the absence of detection of a register access conflict, permitting an instruction to access logical registers via a fixed corresponding physical data registers;

upon detecting a read after write (RAW) register access conflict, stalling an instruction a number of pipeline stages indicated by the stall vector and thereafter permitting the instruction to access logical registers via the physical data registers; and

upon detection of a write after read (WAR) or write after write (WAW) register access conflict, writing data to a shadow register and following expiration of a number of pipeline stages indicated by the stall vector transferring data from the shadow register to the physical data register corresponding to the logical register of a data destination of the instruction.

24. (New) The method of claim 23, wherein the set of shadow registers is less than a maximum number of instructions that can simultaneously cause register access conflicts of instructions between the pipeline stages, the method further comprising the steps of:

upon detection of a write after read (WAR) or write after write (WAW) register access conflict if a shadow register is free

writing data to a shadow register and following expiration of a number of pipeline stages indicated by the stall vector transferring data from the shadow register to the physical data register corresponding to the logical register of a data destination of the instruction, and

freeing the shadow register; and

upon detection of a write after read (WAR) or write after write (WAW) register access conflict if no shadow register is free

stalling an instruction a number of pipeline stages indicated by the stall vector, and

thereafter permitting the instruction to access logical registers via the physical data registers.